said array are electrically isolated by dielectric isolation regions formed in said substrate; and

for each row of memory cells of said array, a conductive member disposed along at least a portion of said row, said conductive member making electrical contact with the source regions of the memory cells of the portion of said row, said conductive member being self-aligned with the memory cells of said portion of said row.

2 1

~~36~~. (New) The non-volatile memory array of claim ~~35~~, and wherein:

said plurality of memory cells includes a first row of memory cells and a second row of memory cells adjacent to the first row, each of the memory cells along a portion of the first row sharing a common source region with at least one memory cell of the second row; and wherein

said conductive member is disposed along at least a portion of the first and second rows, said conductive member making electrical contact with the common source regions of the memory cells in said portion of the first and second rows, the contact of said conductive member being self-aligned with the memory cells of said portion of the first and second rows.

3 1

~~37~~. (New) The non-volatile memory array of claim ~~35~~, and wherein:

said plurality of memory cells includes a plurality of row pairs, at least a portion of the memory cells in each row pair having common source regions; and

a conductive member associated with each row pair, each conductive member being disposed along said portion of its respective row pair and making electrical contact with the common source regions thereof, the contact of each conductive member being self-aligned with the memory cells of said portion of its respective row pair.

4 1

~~38~~. (New) The non-volatile memory array of claim ~~35~~, and wherein:

said memory cells are arranged in a plurality of rows, the control gates of the memory cells in each row being commonly coupled to a corresponding word line that extends generally parallel to the row; and

a conductive member associated with at least one row of memory cells, each conductive member being disposed generally parallel to the corresponding word line along at least a portion of its respective row of memory cells and making electrical contact with the source regions thereof, the contact of each conductive member being self-aligned with the memory cells of said portion of its respective row.

5 ~~39~~. (New) The non-volatile memory array of claim 4 ~~38~~, and wherein:

each said conductive member overlaps the word line of its corresponding row along at least said portion of its corresponding row.

6 ~~40~~. (New) The non-volatile memory array of claim 4 ~~38~~, and wherein:

C1 the plurality of rows includes pairs of adjacent rows, at least a portion of the memory cells of the pairs of adjacent rows sharing common source regions; and wherein

each said conductive member is associated with a pair of adjacent rows, and is disposed generally parallel to the word lines of its respective pair of adjacent rows along at least a portion of its pair of adjacent rows and makes electrical contact with the common source regions thereof, each said conductive member overlapping the word lines of its associated pair of adjacent rows along at least said portion of its respective pair of adjacent rows.

7 ~~41~~. (New) The non-volatile memory array of claim 1 ~~35~~, and wherein:

said conductive member includes polysilicon.

8 ~~42~~. (New) The non-volatile memory array of claim 7 ~~41~~, and wherein:

said conductive member includes a metal silicide.

9 ~~43~~. (New) The non-volatile memory array of claim 7 ~~41~~, and wherein:

said conductive member includes a metal.

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10 1

~~44~~. (New) The nonvolatile memory array of claim ~~35~~, and including:

a plurality of conductive members; and

a source decoder and driving circuit coupled to said conductive members to drive selected conductive members to an erase voltage in response to a plurality of source decode signals.

11 10

~~45~~. (New) The non-volatile memory array of claim ~~44~~, and wherein:

the plurality of source code signals are generated in response to at least one memory address signal.

12 10

~~46~~. (New) The non-volatile memory array of claim ~~44~~, and wherein:

C1 the plurality of source decode signals are generated in response to at least one user determined value.

13

~~47~~. (New) In a flash EPROM memory device formed on a semiconductor substrate, an array configuration comprising:

a plurality of flash EPROM cells arranged in a plurality of rows extending in a row direction and a plurality of columns extending in a column direction; and

a plurality of source connecting members extending in the row direction, each of said source connecting members disposed over and making electrical contact with source regions of memory cells of adjacent pairs of rows, the source regions of memory cells in adjacent columns of said array being electrically isolated by dielectric isolations regions formed in the semiconductor substrate; and

each of said source connecting members enabling the selective erasing of the memory cells of one or both of the corresponding rows during an operation.

14 13

~~48~~. (New) The array configuration of claim ~~47~~, and wherein:

said source connecting members enable the selective erasing of the memory cells of one or more of the row pairs during and erase operation.

15 13
~~49~~. (New) The array configuration of claim ~~47~~, and including:

a plurality of bit line contacts formed along at least one row of the array, opposite to said source connecting members.

16 13
~~50~~. (New) The array configuration of claim ~~47~~, and including:

said source connecting members being double diffused.

17 13
~~51~~. (New) The array configuration of claim ~~47~~, and wherein:

each flash EPROM cell includes a floating gate, the array further including a plurality of word lines each disposed along at least one of the rows, over and insulated from the floating gates of the row; and

said plurality of source connecting members are self-aligned with the said word lines and the floating gates of the rows.

C1

18 13
~~52~~. (New) The array configuration of claim ~~47~~, and comprising:

a plurality of source driver means for coupling at least one source connecting member to an erase voltage in response to a driver input signal; and

a source decoder means for generating at least one driver input signal in response to the source decode signals.

19 18
~~53~~. (New) The array configuration of claim ~~52~~, and including:

address dependent source decode signal generating means responsive to a plurality of memory address signals for generating the source decode signals.

20 18
~~54~~. (New) The array configuration of claim ~~52~~, and including:

user dependent source decode signal generating means responsive to a plurality of predefined user values for generating the source decode signals.

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21 18
~~55~~. (New) The array configuration of claim ~~52~~, and including:

configurable source decode signal generating means responsive to a plurality of predefined user values and memory address values for generating the source decode signals.

22
~~56~~. (New) A non-volatile memory array formed in a semiconductor substrate, comprising:

a plurality of memory cells arranged in at least a first row of memory cells and a second row of memory cells adjacent to the first row, thereby forming adjacent columns of memory cells, each of the memory cells along a portion of the first row sharing a common source region with at least one memory cell of the second row; and

C1

a conductive member being disposed along at least a portion of the first and second rows, said conductive member being associated with the first and second rows and making electrical contact with the common source regions of the memory cells in said portion of the rows, the contact of said conductive member being self-aligned with the memory cells of said portion of the rows, and

wherein said conductive member enables the selection of the one of the first or second rows during an erase operation, and

wherein the source regions of adjacent columns of memory cells are electrically isolated by dielectric isolation regions formed in the semiconductor substrate.

23 22
~~57~~. (New) The non-volatile memory array of claim ~~56~~, and wherein each of said memory cells includes a drain region, a source region, a channel region disposed between the drain region and the source region, a floating gate disposed over at least the channel region, and a control gate disposed over the floating gates, the control gates of the memory cell in each row being commonly coupled to a word line extending generally parallel to the row, the conductive member being disposed generally parallel to the word line along at least portion of its respective row.

C